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Compact Modeling POWER/HVMOS Devices Compact Modeling Compact Modeling of Circuits and Devices in Verilog-A Compact Models for Integrated Circuit Design *Floating Gate Devices: Operation and Compact Modeling PHYSICS-BASED COMPACT MODELING OF ORGANIC ELECTRONIC DEVICES FinFET Modeling for IC Simulation and Design* Open Source TCAD/EDA for Compact Modeling Mosfet Modeling for VLSI Simulation **Industry Standard FDSOI Compact Model BSIM-IMG for IC Design Compact Modeling of Variability in RRAM Devices and Its Impact on Neuromorphic Circuit Applications Compact Modeling of Spintronic Devices** Compact Modeling of Silicon Carbide Junction Field Effect Devices **Process-based Compact Modeling and Analysis of Silicon-on-insulator CMOS Devices and Circuits, Including Double-gate MOSFETS** Compact Modeling of Gallium Nitride Power Semiconductor Devices for Advanced Power Electronics Design Numerical and Compact Modeling of Embedded Flash Memory Devices Targeted for IC Design **Physics-based Compact Modeling of Valence-change-based Resistive Switching Devices** Compact Models for Integrated Circuit Design **Methods for Compact Modeling of Process Variations in Silicon Photonics Devices** *Compact Transistor Modelling for Circuit Design* **Compact modeling of multiple gate MOS devices[** Application of Advanced Optimization and Expert System Approaches to Compact Modeling of Semiconductor Devices *Compact Transistor Modelling for Circuit Design* Compact Hierarchical Bipolar Transistor Modeling with Hicum Compact Modeling of the RF and Noise Behavior of Multiple-Gate MOSFETs **Compact Modeling of Multi Gate and Other Emerging Transistors** Compact Modeling of Thin-film Silicon Transistors Fabricated on Glass Resistive Random Access Memory (RRAM) **FinFET/GAA Modeling for IC Simulation and Design A Practical Guide to Verilog-A** Compact Modeling of Nanoscale CMOS *Design, Characterization and Compact Modeling of Novel Silicon Controlled Rectifier (SCR)-based Devices for Electrostatic Discharge (ESD) Protection Applications in Integrated Circuits Compact Extended Linear Programming Models Introducing Technology Computer-Aided Design (TCAD)* **MOSFET Modeling for Circuit Analysis and Design Compact Modeling of Double-Gate MOSFETs** *Compact MOSFET Models for VLSI Design Modeling of III-V Nanoscale Field-effect Transistors for Logic Circuits* **NQS Effects Investigation For Compact Bipolar Transistor Modeling** BSIM4 and MOSFET Modeling For IC Simulation

FinFET/GAA Modeling for IC Simulation and Design: Using the BSIM-CMG Standard, Second Edition is the first to book to explain FinFET modeling for IC simulation and the industry standard - BSIM-CMG - describing the rush in demand for advancing the technology from planar to 3D architecture as now enabled by the approved industry standard. The book gives a strong foundation on the physics and operation of FinFET, details aspects of the BSIM-CMG model such as surface potential, charge and current calculations, and includes a dedicated chapter on parameter extraction procedures, thus providing a step-by-step approach for the efficient extraction of model parameters. With this book, users will learn Why you should use FinFET, The physics and operation of FinFET Details of the FinFET standard model (BSIM-CMG), Parameter extraction in BSIM-CMG FinFET circuit design and simulation, and more. Industry Standard FDSOI Compact Model BSIM-IMG for IC Design helps readers develop an understanding of a FDSOI device and its simulation model. It covers the physics and operation of the FDSOI device, explaining not only how FDSOI enables further scaling, but also how it offers unique possibilities in circuits. Following chapters cover the industry standard compact model BSIM-IMG for FDSOI devices. The book addresses core surface-potential calculations and the plethora of real devices and potential effects. Written by the original developers of the industrial standard model, this book is an excellent reference for the new BSIM-IMG compact model for emerging FDSOI technology. The authors include chapters on step-by-step parameters extraction procedure for BSIM-IMG model and rigorous industry grade tests that the BSIM-IMG model has undergone. There is also a chapter on analog and RF circuit design in FDSOI technology using the BSIM-IMG model. Provides a detailed discussion of the BSIM-IMG model and the industry standard simulation model for FDSOI, all presented by the developers of the model Explains the complex operation of the FDSOI device and its use of two independent control inputs Addresses the parameter extraction challenges for those using this model This book provides a handy, unified introduction to the theory of compact extended formulations of exponential-size integer linear programming (ILP) models. Compact extended formulations are equally powerful, but polynomial-sized, models whose solutions do not require the implementation of separation and pricing procedures. The book is written in a general, didactic form, first developing the background theoretical concepts (polyhedra, projections, linear and integer programming) and then delving into the various techniques for compact extended reformulations. The techniques are illustrated through a wealth of examples touching on many application areas, such as classical combinatorial optimization, network design, timetabling, scheduling, routing, computational biology and bioinformatics. The book is intended for graduate or PhD students – either as an advanced course on selected topics or within a more general course on ILP and mathematical programming – as well as for practitioners and software engineers in industry exploring techniques for developing optimization models for their specific problems. Practicing designers, students, and educators in the semiconductor field face an ever expanding portfolio of MOSFET models. In Compact MOSFET Models for VLSI Design , A.B. Bhattacharyya presents a unified perspective on the topic, allowing the practitioner to view and interpret device phenomena concurrently using different modeling strategies. Readers will learn to link device physics with model parameters, helping to close the gap between device understanding and its use for optimal

circuit performance. Bhattacharyya also lays bare the core physical concepts that will drive the future of VLSI development, allowing readers to stay ahead of the curve, despite the relentless evolution of new models. Adopts a unified approach to guide students through the confusing array of MOSFET models Links MOS physics to device models to prepare practitioners for real-world design activities Helps fabless designers bridge the gap with off-site foundries Features rich coverage of: quantum mechanical related phenomena Si-Ge strained-Silicon substrate non-classical structures such as Double Gate MOSFETs Presents topics that will prepare readers for long-term developments in the field Includes solutions in every chapter Can be tailored for use among students and professionals of many levels Comes with MATLAB code downloads for independent practice and advanced study This book is essential for students specializing in VLSI Design and indispensible for design professionals in the microelectronics and VLSI industries. Written to serve a number of experience levels, it can be used either as a course textbook or practitioner's reference. Access the MATLAB code, solution manual, and lecture materials at the companion website: www.wiley.com/go/bhattacharyya Photonic systems are being developed with extensions to existing CMOS processes, and are growing in complexity. Silicon photonics designs are evaluated in simulation using similar methods to those used for CMOS transistor and circuit designs; simulation models for common silicon-based photonics structures and devices currently exist and are used to design larger photonic systems. However, these photonics models are often not constructed with manufacturing variations in mind. This thesis presents methods for creating simulation models for nanophotonic devices that take systematic and random variations from manufacturing into account. Factorial experiment design is used to explore the eect of process variations on photonic device performance. Corner models are constructed using the results from experiment design and capture worst-case variations. The response surface modeling method is employed to develop parameterized compact models. Example variation-aware compact models are generated using these methods for the directional coupler and the Y-branch, two passive devices widely used in silicon photonics. The use of these models is demonstrated through corner and statistical variation analyses of a simple Mach-Zehnder interferometer photonic circuit composed of the directional coupler and Y-branch devices. Floating Gate Devices: Operation and Compact Modeling focuses on standard operations and compact modeling of memory devices based on Floating Gate architecture. Floating Gate devices are the building blocks of Flash, EPROM, EEPROM memories. Flash memories, which are the most versatile nonvolatile memories, are widely used to store code (BIOS, Communication protocol, Identification code,) and data (solid-state Hard Disks, Flash cards for digital cameras,). The reader, who deals with Floating Gate memory devices at different levels - from test-structures to complex circuit design - will find an essential explanation on device physics and technology, and also circuit issues which must be fully understood while developing a new device. Device engineers will use this book to find simplified models to design new process steps or new architectures. Circuit designers will find the basic theory to understand the use of compact models to validate circuits against process variations and to evaluate the impact of parameter variations on circuit performances. Floating Gate Devices: Operation and Compact Modeling is meant to be a basic tool for designing the next generation of memory devices based on FG technologies. Semiconductor power electronics plays a dominant role due its increased efficiency and high reliability in various domains including the medium and high electrical drives, automotive and aircraft applications, electrical power conversion, etc. Power/HVMOS Devices Compact Modeling will cover very extensive range of topics related to the development and characterization power/high voltage (HV) semiconductor technologies as well as modeling and simulations of the power/HV devices and smart power integrated circuits (ICs). Emphasis is placed on the practical applications of the advanced semiconductor technologies and the device level compact/spice modeling. This book is intended to provide reference information by selected, leading authorities in their domain of expertise. They are representing both academia and industry. All of them have been chosen because of their intimate knowledge of their subjects as well as their ability to present them in an easily understandable manner. Modern high speed (RF) transistors encounter certain delay while operated at high frequency or under fast transient condition. This effect is named as Non Quasi Static (NQS) effect. In this work, NQS effect is analyzed in a concise manner so that it can be readily implemented in a compact model using the VerilogA description language. The basic physics behind this effect is investigated in small signal domain and results are compared with the published work. Compact modeling with HICUM model is performed with both measured and device simulated data. At last, an improved excess phase circuit is proposed to model the NQS effect. RRAM technology has made significant progress in the past decade as a competitive candidate for the next generation non-volatile memory (NVM). This lecture is a comprehensive tutorial of metal oxide-based RRAM technology from device fabrication to array architecture design. State-of-the-art RRAM device performances, characterization, and modeling techniques are summarized, and the design considerations of the RRAM integration to large-scale array with peripheral circuits are discussed. Chapter 2 introduces the RRAM device fabrication techniques and methods to eliminate the forming process, and will show its scalability down to sub-10 nm regime. Then the device performances such as programming speed, variability control, and multi-level operation are presented, and finally the reliability issues such as cycling endurance and data retention are discussed. Chapter 3 discusses the RRAM physical mechanism, and the materials characterization techniques to observe the conductive filaments and the electrical characterization techniques to study the electronic conduction processes. It also presents the numerical device modeling techniques for simulating the evolution of the conductive filaments as well as the compact device modeling techniques for circuit-level design. Chapter 4 discusses the two common RRAM array architectures for large-scale integration: one-transistor-one-resistor (1T1R) and cross-point architecture with selector. The write/read schemes are presented and the peripheral circuitry design considerations are discussed. Finally, a 3D integration approach is introduced for building ultra-high density RRAM array. Chapter 5 is a brief summary and will give an outlook for RRAM's potential novel applications beyond the NVM applications. "The semiconductor industry, now entering its seventh decade, continues to innovate and evolve at a breakneck pace. E.O. Wilson, the famous Harvard biologist who is an expert on ants, estimates that there are 1017 ants on earth. The semiconductor industry is now shipping 100 transistors per ant every year. In addition, the pace of growth means we are building more electronics in a year than existed on January 1st of that year! A major driver for this growth in recent years is the portable consumer electronics market which includes cell phones, personal digital assistants, and tablets. The focus of this dissertation is centered on a new thin-film silicon technology on glass introduced by Corning Inc., and targeted to meet the needs of the portable product display market. The work presented in this dissertation revolves around a new technology developed by Corning Inc. known as Silicon on Glass of SiOG which permits the transfer of a thin single-crystal silicon film to a glass substrate. This technology coupled with a low-temperature CMOS process has the potential to create devices with performance characteristics rivaling those developed using conventional bulk CMOS processes. These higher performing devices

permit an increased level of circuit integration directly on the glass substrate and have the potential to enable new display technologies such as OLED (Organic Light Emitting Diode). The SiOG CMOS devices are distinctly different from traditional thin-film, silicon-on-insulator, and bulk CMOS devices in that they rely on both surface and bulk conduction. Furthermore, their current-voltage characteristics are heavily influenced by fringing electric fields in the glass substrate. This dissertation presents an overview of display technology as well as a review of computer-aided design tools for integrated circuit development with a focus on compact modeling. In addition, some early work on developing advanced OLED display driver circuits using SiOG technology is presented. The bulk of this dissertation is focused on the development of compact models which properly describe the electrical characteristics of SiOG CMOS devices. For all but the most trivial cases, the set of coupled nonlinear partial differential equations that describe semiconductor device behavior has not been solved analytically. Even when the semiconductor equations that represent current flow, charge distribution, and potential distribution are decoupled and device-specific simplifications are applied, analytic solutions remain elusive. Two different methods for developing compact models for the SiOG CMOS devices are presented with distinct methods for developing approximate solutions. In addition, a model for the fringing electric field is developed using conformal mapping techniques, and its effect on drain current is explored. Finally, a new technique for solving the nonlinear semiconductor equations is explored. The application of a new mathematical technique known as the Homotopy Analysis Method (HAM) is presented as it relates to the general Poisson's equation for semiconductor devices."--Abstract. Electrostatic Discharge (ESD), an event of a sudden transfer of electrons between two bodies at different potentials, happens commonly throughout nature. When such even occurs on integrated circuits (ICs), ICs will be damaged and failures result. As the evolution of semiconductor technologies, increasing usage of automated equipments and the emerging of more and more complex circuit applications, ICs are more sensitive to ESD strikes. Main ESD events occurring in semiconductor industry have been standardized as human body model (HBM), machine model (MM), charged device model (CDM) and international electrotechnical commission model (IEC) for control, monitor and test. In additional to the environmental control of ESD events during manufacturing, shipping and assembly, incorporating on-chip ESD protection circuits inside ICs is another effective solution to reduce the ESD-induced damage. This dissertation presents design, characterization, integration and compact modeling of novel silicon controlled rectifier (SCR)-based devices for on-chip ESD protection. The SCR-based device with a snapback characteristic has long been used to form a V[subscript SS]-based protection scheme for on-chip ESD protection over a broad rang of technologies because of its low on-resistance, high failure current and the best area efficiency. The ESD design window of the snapback device is defined by the maximum power supply voltage as the low edge and the minimum internal circuitry breakdown voltage as the high edge. The downscaling of semiconductor technology keeps on squeezing the design window of on-chip ESD protection. For the submicron process and below, the turn-on voltage and sustain voltage of ESD protection cell should be lower than 10 V and higher than 5 V, respectively, to avoid core circuit damages and latch-up issue. This presents a big challenge to device/circuit engineers. Meanwhile, the high voltage technologies push the design window to another tough range whose sustain voltage, 45 V for instance, is hard for most snapback ESD devices to reach. Based on the in-depth elaborating on the principle of SCR-based devices, this dissertation first presents a novel unassisted, low trigger- and high holding-voltage SCR (uSCR) which can fit into the aforesaid ESD design window without involving any extra assistant circuitry to realize an area-efficient on-chip ESD protection for low voltage applications. The on-chip integration case is studied to verify the protection effectiveness of the design. Subsequently, this dissertation illustrate the development of a new high holding current SCR (HHC-SCR) device for high voltage ESD protection with increasing the sustain current, not the sustain voltage, of the SCR device to the latchup-immune level to avoid sacrificing the ESD protection robustness of the device. The ESD protection cells have been designed either by using technology computer aided design (TCAD) tools or through trial-and-error iterations, which is cost- or time-consuming or both. Also, the interaction of ESD protection cells and core circuits need to be identified and minimized at pre-silicon stage. It is highly desired to design and evaluate the ESD protection cell using simulation program with integrated circuit emphasis (SPICE)-like circuit simulation by employing compact models in circuit simulators. And the compact model also need to predict the response of ESD protection cells to very fast transient ESD events such as CDM event since it is a major ESD failure mode. The compact model for SCR-based device is not widely available. This dissertation develops a macromodeling approach to build a comprehensive SCR compact model for CDM ESD simulation of complete I/O circuit. This modeling approach offers simplicity, wide availability and compatibility with most commercial simulators by taking advantage of using the advanced BJT model, Vertical Bipolar Inter-Company (VBIC) model. SPICE Gummel-Poon (SGP) model has served the ICs industry well for over 20 years while it is not sufficiently accurate when using SGP model to build a compact model for ESD protection SCR. This dissertation seeks to compare the difference of SCR compact model built by using VBIC and conventional SGP in order to point out the important features of VBIC model for building an accurate and easy-CAD implement SCR model and explain why from device physics and model theory perspectives. This might be the first book that deals mostly with the 3D technology computer-aided design (TCAD) simulations of major state-of-the-art stress- and strain-engineered advanced semiconductor devices: MOSFETs, BJTs, HBTs, nonclassical MOS devices, finFETs, silicon-germanium hetero-FETs, solar cells, power devices, and memory devices. The book focuses on how to set up 3D TCAD simulation tools, from mask layout to process and device simulation, including design for manufacturing (DFM), and from device modeling to SPICE parameter extraction. The book also offers an innovative and new approach to teaching the fundamentals of semiconductor process and device design using advanced TCAD simulations of various semiconductor structures. The simulation examples chosen are from the most popular devices in use today and provide useful technology and device physics insights. To extend the role of TCAD in today’s advanced technology era, process compact modeling and DFM issues have been included for design–technology interface generation. Unique in approach, this book provides an integrated view of silicon technology and beyond—with emphasis on TCAD simulations. It is the first book to provide a web-based online laboratory for semiconductor device characterization and SPICE parameter extraction. It describes not only the manufacturing practice associated with the technologies used but also the underlying scientific basis for those technologies. Written from an engineering standpoint, this book provides the process design and simulation background needed to understand new and future technology development, process modeling, and design of nanoscale transistors. The book also advances the understanding and knowledge of modern IC design via TCAD, improves the quality in micro- and nanoelectronics R&D, and supports the training of semiconductor specialists. It is intended as a textbook or reference for graduate students in the field of semiconductor fabrication and as a reference for engineers involved in VLSI technology development who

have to solve device and process problems. CAD specialists will also find this book useful since it discusses the organization of the simulation system, in addition to presenting many case studies where the user applies TCAD tools in different situations. During the first decade following the invention of the transistor, progress in semiconductor device technology advanced rapidly due to an effective synergy of technological discoveries and physical understanding. Through physical reasoning, a feeling for the right assumption and the correct interpretation of experimental findings, a small group of pioneers conceived the major analytic design equations, which are currently to be found in numerous textbooks. Naturally with the growth of specific applications, the description of some characteristic properties became more complicated. For instance, in inte grated circuits this was due in part to the use of a wider bias range, the addition of inherent parasitic elements and the occurrence of multi dimensional effects in smaller devices. Since powerful computing aids became available at the same time, complicated situations in complex configurations could be analyzed by useful numerical techniques. Despite the resulting progress in device optimization, the above approach fails to provide a required compact set of device design and process control rules and a compact circuit model for the analysis of large-scale electronic designs. This book therefore takes up the original thread to some extent. Taking into account new physical effects and introducing useful but correct simplifying assumptions, the previous concepts of analytic device models have been extended to describe the characteristics of modern integrated circuit devices. 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With the advent of multi gate and nanoscale fabrication techniques, several new transistor topographies have been proposed and manufactured in the past decade. In parallel, accurate and efficient compact models for these devices have been likewise developed. This paper summarizes the major topographies and their associated compact models with a focus toward computationally efficient models constructed for implementation in common modeling languages such as Verilog-A and SPICE. Common physical and mathematical modeling techniques have also been reviewed as has the evolution from simple multi gate devices to nanoscale structures. Discover how Verilog-A is particularly designed to describe behavior and connectivity of circuits and system components for analog SPICE-class simulators, or for continuous time (SPICE-based) kernels in Verilog-AMS simulators. With continuous updates since it’s release 30 years ago, this practical guide provides a comprehensive foundation and understanding to the modeling language in its most recent standard formulation. With the introduction of language extensions to support compact device modeling, the Verilog-A has become today de facto standard language in the electronics industry for coding compact models of active and passive semiconductor devices. You'll gain an in depth look at how analog circuit simulators work, solving system equations, modeling of components from other physical domains, and modeling the same physical circuits and systems at various levels of detail and at different levels of abstraction. All industry standard compact models released by Si2 Compact Model Coalition (CMC) as well as compact models of emerging nano-electronics devices released by New Era Electronic Devices and Systems (NEEDS) initiative are coded in Verilog-A. This book prepares you for the current trends in the neuromorphic computing, hardware customization for artificial intelligence applications as well as circuit design for internet of things (IOT) will only increase the need for analog simulation modeling and make Verilog-A even more important as a multi-domain component-oriented modeling language. Let A Practical Guide to Verilog-A be the initial step in learning the extended mixed-signal Verilog-AMS hardware description language. What You'll Learn Review the hardware description and modeling language Verilog-A in its most recent standard formulation. Code new compact models of active and passive semiconductor devices as well as new models for emerging circuit components from different physical disciplines. Extend the application of SPICE-like circuit simulators to non-electronics field (neuromorphic, thermal, mechanical, etc systems). Apply the initial steps towards the extended mixed-signal Verilog-AMS hardware description language. Who This Book Is For Electronic circuit designers and SPICE simulation model developers in academia and industry. Developers of electronic design automation (EDA) tools. Engineers, scientists and students of various disciplines using SPICE-like simulators for research and development. This book is the first to explain FinFET modeling for IC simulation and the industry standard – BSIM-CMG - describing the rush in demand for advancing the technology from planar to 3D architecture, as now enabled by the approved industry standard. The book gives a strong foundation on the physics and operation of FinFET, details aspects of the BSIM-CMG model such as surface potential, charge and current calculations, and includes a dedicated chapter on parameter extraction procedures, providing a step-by-step approach for the efficient extraction of model parameters. With this book you will learn: Why you should use FinFET The physics and operation of FinFET Details of the FinFET standard model (BSIM-CMG) Parameter extraction in BSIM-CMG FinFET circuit design and simulation Authored by the lead inventor and developer of FinFET, and developers of the BSIM-CM standard model, providing an experts’ insight into the specifications of the standard The first book on the industry-standard FinFET model - BSIM-CMG This is the first book dedicated to the next generation of MOSFET models. Addressed to circuit designers with an in-depth treatment that appeals to device specialists, the book presents a fresh view of compact modeling, having completely abandoned the regional modeling approach.Both an overview of the basic physics theory required to build compact MOSFET models and a unified treatment of inversion-charge and surface-potential models are provided. The needs of digital, analog and RF designers as regards the availability of simple equations for circuit designs are taken into account. Compact expressions for hand analysis or for automatic synthesis, valid in all operating regions, are presented throughout the book. All the main expressions for computer simulation used in the new generation compact models are derived.Since

designers in advanced technologies are increasingly concerned with fluctuations, the modeling of fluctuations is strongly emphasized. A unified approach for both space (matching) and time (noise) fluctuations is introduced. The nanoelectronics world is moving forward at incredible speed, and technology keeps improving overnight. One can no longer afford to spend months or even years evaluating a future technological node, thus the need for a robust evaluation system has arisen. Numerical ways of modeling the new device architectures, apart from precision, offer very little in terms of performance, and are being replaced by new analytical tools, focus on providing exactly that - speed and accuracy. This work has been conceived to cover precisely these aspects. The models described here are physical models, with very few adjustment parameters, that are usually replaceable with values extracted from experimental measurements. They have the advantage of being easily incorporated into circuit simulators, which allow designers to unleash the full capabilities of the design software to create new devices and applications. The aim of this book is to highlight the benefits of a higher interoperability between Technology Computer-Aided Design and Electronic Design Automation, focusing on specifically selected open source tools for compact modeling. Due to the tremendous developments in semiconductor technology in recent years, device level modelling and integrated circuit design have become intimately related. However, they have been traditionally disconnected up to the circuit level. This book consists of a set of extended user manuals guiding the reader from the usual software, from multidimensional numerical process and device simulations, through compact model development and its Verilog-A standardization to carefully selected IC designs for analog, radio frequency and digital applications. Bringing together contributions from academic and industrial researchers and engineers, the book forms a valuable reference for students and those working in the field. The compact model of a circuit or device is a system of linear and/or nonlinear differential equations that effectively models the behavior of the circuit or device. Compact modeling plays a critical role in circuit simulation, because in order to simulate a circuit with a specific component, the compact model of this component is needed in the circuit simulator. Two contributions related to compact modeling in Verilog-A are presented in this thesis. The first contribution is an analysis of the feasibility and performance of the Verilog-A language in the context of implementing reduced order models. Reduced order models are a class of purely mathematical compact models, which are significantly faster than compact models based on the physics of a device or system. The second contribution of this thesis is the implementation of a novel MOSFET model in Verilog-A. This MOSFET model is known as the Virtual Source model. As silicon CMOS technology continues to scale down its minimum critical dimension, it becomes increasingly difficult to enhance device switching speed due to fundamental limitations. Innovations in device structure and materials are pursued to accommodate improvement in performance as well as reduction in transistor size. For beyond-22-nm CMOS technology, III-V channel FETs are considered as a compelling candidate for extending the device scaling limit of low-power and high-speed operation, owing to their superb carrier transport properties and recent experimental advancements. In this thesis, device simulation, compact modeling, circuit design, circuit performance assessment and estimation of III-V logic transistors are carried out to study key considerations such as device pitch, parasitics, and the importance of PMOS for circuit-level performance. To effectively connect device characteristics with circuit design, a physics-based compact model for digital logic is constructed. The model encompasses effects such as field-confined and spatially-confined trapezoidal quantum well sub-band energies, gate leakage tunneling current and parasitic capacitance. The developed compact model contains only three fitting parameters and is verified by experiment and circuit simulations. The compact model enables other bodies of work for the purpose of circuit-level design and performance estimation. To demonstrate the capability of the model in a circuit environment we apply the compact model to composite circuits such as FO4 inverter chains and SRAM cache to evaluate and project performance and power trends for beyond-22-nm technology. Compact Hierarchical Bipolar Transistor Modeling with HICUM will be of great practical benefit to professionals from the process development, modeling and circuit design community who are interested in the application of bipolar transistors, which include the SiGe:C HBTs fabricated with existing cutting-edge process technology. The book begins with an overview on the different device designs of modern bipolar transistors, along with their relevant operating conditions; while the subsequent chapter on transistor theory is subdivided into a review of mostly classical theories, brought into context with modern technology, and a chapter on advanced theory that is required for understanding modern device designs. This book aims to provide a solid basis for the understanding of modern compact models. Gallium Nitride is a relatively new material compound compared to Silicon that has demonstrated immense promise as a material for power semiconductor devices. Silicon based power semiconductor devices have already reached very close their theoretical limits and it may not be possible to extract any further efficiency improvements out of these devices. Lateral GaN devices have already penetrated the power electronics market with breakdown voltages up to 650 V. Theoretically, gallium nitride has already demonstrated excellent figure of merit compared to silicon and silicon carbide. Currently, compact models that can predict the performance characteristics of a wide range of lateral GaN devices are not readily available. The models currently available are semi-empirical/empirical SPICE models or physical models for RF GaN devices. This work presents a compact GaN device model that can predict the performance characteristics of a wide range of commercial GaN devices. The model has been validated against the characteristics of medium voltage-range EPC devices and high-voltage range Panasonic GaN devices. The medium-voltage range devices do not have any significant drift resistance in their on-state behavior while the high-voltage range devices exhibit significant non-linear drift resistance which is evident from their on-state behavior. The medium-voltage range devices have non-linear reverse capacitance due to the depletion region. The high-voltage GaN device have significant non-linear capacitance behavior due to the existence of field-plates connected to the source and drain. The field-plates are fabricated to augment the electric-field distribution in the channel. However, field plates result in significant non-linearity in the channel which can be seen as successive depletion in the device capacitances. These effects are accurately characterized by the proposed model in this work. The model also captures the third-quadrant behavior of all GaN devices with the model parameters that are de-coupled from the first quadrant while maintaining continuity between the first and third quadrant. The model also captures the temperature dependent device characteristics. The convergence capability of the model is also verified using various power electronics topologies. Most of the recent texts on compact modeling are limited to a particular class of semiconductor devices and do not provide comprehensive coverage of the field. Having a single comprehensive reference for the compact models of most commonly used semiconductor devices (both active and passive) represents a significant advantage for the reader. Indeed, several kinds of semiconductor devices are routinely encountered in a single IC design or in a single modeling support group. Compact Modeling includes mostly the material that after several years of IC design applications has been found both theoretically sound and practically significant. Assigning the individual chapters to the groups responsible for the definitive work on the subject assures

the highest possible degree of expertise on each of the covered models. Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond provides a modern treatise on compact models for circuit computer-aided design (CAD). Written by an author with more than 25 years of industry experience in semiconductor processes, devices, and circuit CAD, and more than 10 years of academic experience in teaching compact modeling courses, this first-of-its-kind book on compact SPICE models for very-large-scale-integrated (VLSI) chip design offers a balanced presentation of compact modeling crucial for addressing current modeling challenges and understanding new models for emerging devices. Starting from basic semiconductor physics and covering state-of-the-art device regimes from conventional micron to nanometer, this text: Presents industry standard models for bipolar-junction transistors (BJTs), metal-oxide-semiconductor (MOS) field-effect-transistors (FETs), FinFETs, and tunnel field-effect transistors (TFETs), along with statistical MOS models Discusses the major issue of process variability, which severely impacts device and circuit performance in advanced technologies and requires statistical compact models Promotes further research of the evolution and development of compact models for VLSI circuit design and analysis Supplies fundamental and practical knowledge necessary for efficient integrated circuit (IC) design using nanoscale devices Includes exercise problems at the end of each chapter and extensive references at the end of the book Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond is intended for senior undergraduate and graduate courses in electrical and electronics engineering as well as for researchers and practitioners working in the area of electron devices. However, even those unfamiliar with semiconductor physics gain a solid grasp of compact modeling concepts from this book. A reprint of the classic text, this book popularized compact modeling of electronic and semiconductor devices and components for college and graduate-school classrooms, and manufacturing engineering, over a decade ago. The first comprehensive book on MOS transistor compact modeling, it was the most cited among similar books in the area and remains the most frequently cited today. The coverage is device-physics based and continues to be relevant to the latest advances in MOS transistor modeling. This is also the only book that discusses in detail how to measure device model parameters required for circuit simulations. The book deals with the MOS Field Effect Transistor (MOSFET) models that are derived from basic semiconductor theory. Various models are developed, ranging from simple to more sophisticated models that take into account new physical effects observed in submicron transistors used in today's (1993) MOS VLSI technology. The assumptions used to arrive at the models are emphasized so that the accuracy of the models in describing the device characteristics are clearly understood. Due to the importance of designing reliable circuits, device reliability models are also covered. Understanding these models is essential when designing circuits for state-of-the-art MOS ICs. Spintronics is an area of electronics that studies the design of electronic devices based on the spin properties of electrons, taking advantage of their full potential. To date, despite the extended theoretical work done on this class of components, models are mainly physical and, due to their extreme complexity, cannot be implemented in circuit simulators. The aim of this work is to address the critical problems of modeling spintronic devices in a compact form. The main goal is to make a bridge between a purely physical description and a more electrical counterpart of spintronic elements in order to enable their use in Computer Assisted Design tools, just as for CMOS devices. The first part of the book gives an introduction to the different kinds of spin-orbit interactions, the materials used for realizing spintronic devices and the main spin-based devices currently developed. The second part is then dedicated to the modeling of simple transistor structures where the current depends on spin-polarized carriers. Moreover, a brief outlook on possible future spintronic devices is given. Double-Gate (DG) MOSFET is a newly emerging device that can potentially further scale down CMOS technology owing to its excellent control of short channel effects. Currently, much research effort is devoted to the development of DG MOSFETs. This dissertation focuses on the compact modeling of DG MOSFETs, aiming to extract the physics of DG MOSFETs and provide a tool for simulating DG MOSFET circuits. We start from the basic Poisson's equation and current continuity equation to rigorously derive the long-channel drain current model without the charge sheet approximation. The model is based on an analytical solution to the potential distribution at any point in the DG MOSFET. It employs one single equation to cover all the operation regions: linear, saturation, and subthreshold, continuously with no fitting parameter. Volume inversion, a non-charge-sheet phenomenon in symmetric DG MOSFETs, is accurately captured by the model. For AC and transient simulations, analytical charge and capacitance models are developed. Both symmetric and asymmetric DG MOSFET models are verified by extensive two dimensional numerical simulations. For small-geometry devices, compact models of the physical phenomena such as short channel effects are developed. In the development of the compact models, special attention is paid to ensure the model is symmetric and continuous in all the operation regions. Quantum effect is also incorporated in the long channel core model. As body doping may be needed to adjust the threshold voltage, we also studied the body doping effect on DG MOSFET and concluded that lightly doped DG MOSFETs can be modeled by adding a threshold voltage shift to the undoped DG MOSFET model. The model has been implemented into SPICE3 and Verilog-A platforms so that it can be used by circuit designers. In the implementation, Newton method is used for solving an implicit equation in the calculation of drain current. We also calibrated the model with respect to the published hardware data to affirm its consistency with the experimental I-V curves. Finally, the model has been released in public domain http://taur.ucsd.edu/~hlu for circuit simulation. Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond provides a modern treatise on compact models for circuit computer-aided design (CAD). Written by an author with more than 25 years of industry experience in semiconductor processes, devices, and circuit CAD, and more than 10 years of academic experience in teaching compact modeling courses, this first-of-its-kind book on compact SPICE models for very-large-scale-integrated (VLSI) chip design offers a balanced presentation of compact modeling crucial for addressing current modeling challenges and understanding new models for emerging devices. Starting from basic semiconductor physics and covering state-of-the-art device regimes from conventional micron to nanometer, this text: Presents industry standard models for bipolar-junction transistors (BJTs), metal-oxide-semiconductor (MOS) field-effect-transistors (FETs), FinFETs, and tunnel field-effect transistors (TFETs), along with statistical MOS models Discusses the major issue of process variability, which severely impacts device and circuit performance in advanced technologies and requires statistical compact models Promotes further research of the evolution and development of compact models for VLSI circuit design and analysis Supplies fundamental and practical knowledge necessary for efficient integrated circuit (IC) design using nanoscale devices Includes exercise problems at the end of each chapter and extensive references at the end of the book Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond is intended for senior undergraduate and graduate courses in electrical and electronics engineering as well as for researchers and practitioners working in the area of electron devices. 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